

FIG. 1

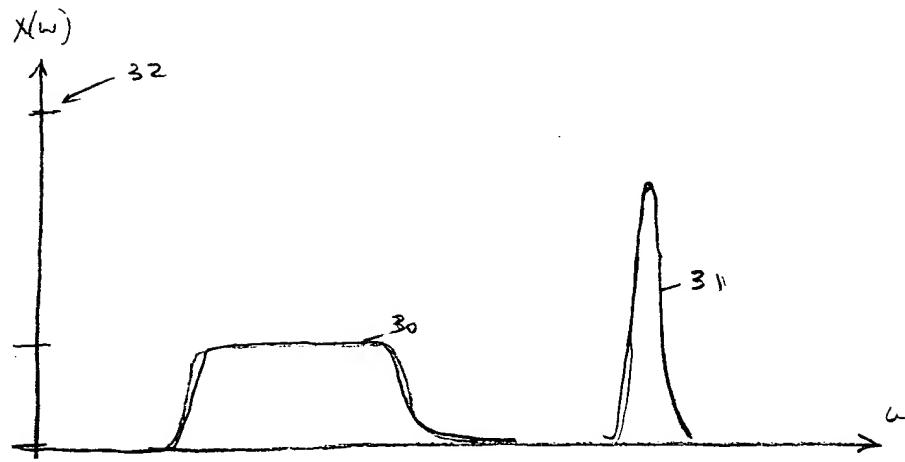


FIG. 2

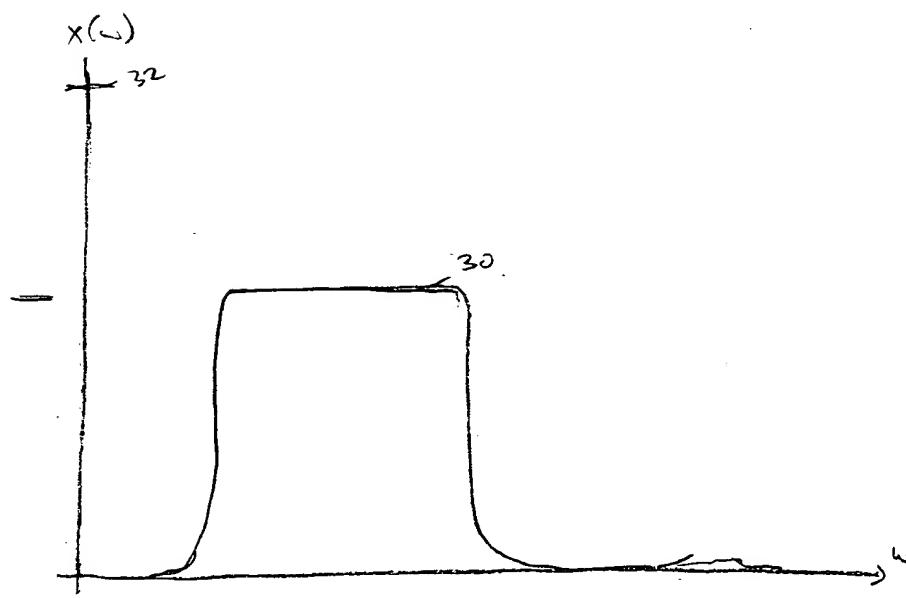


FIG. 3

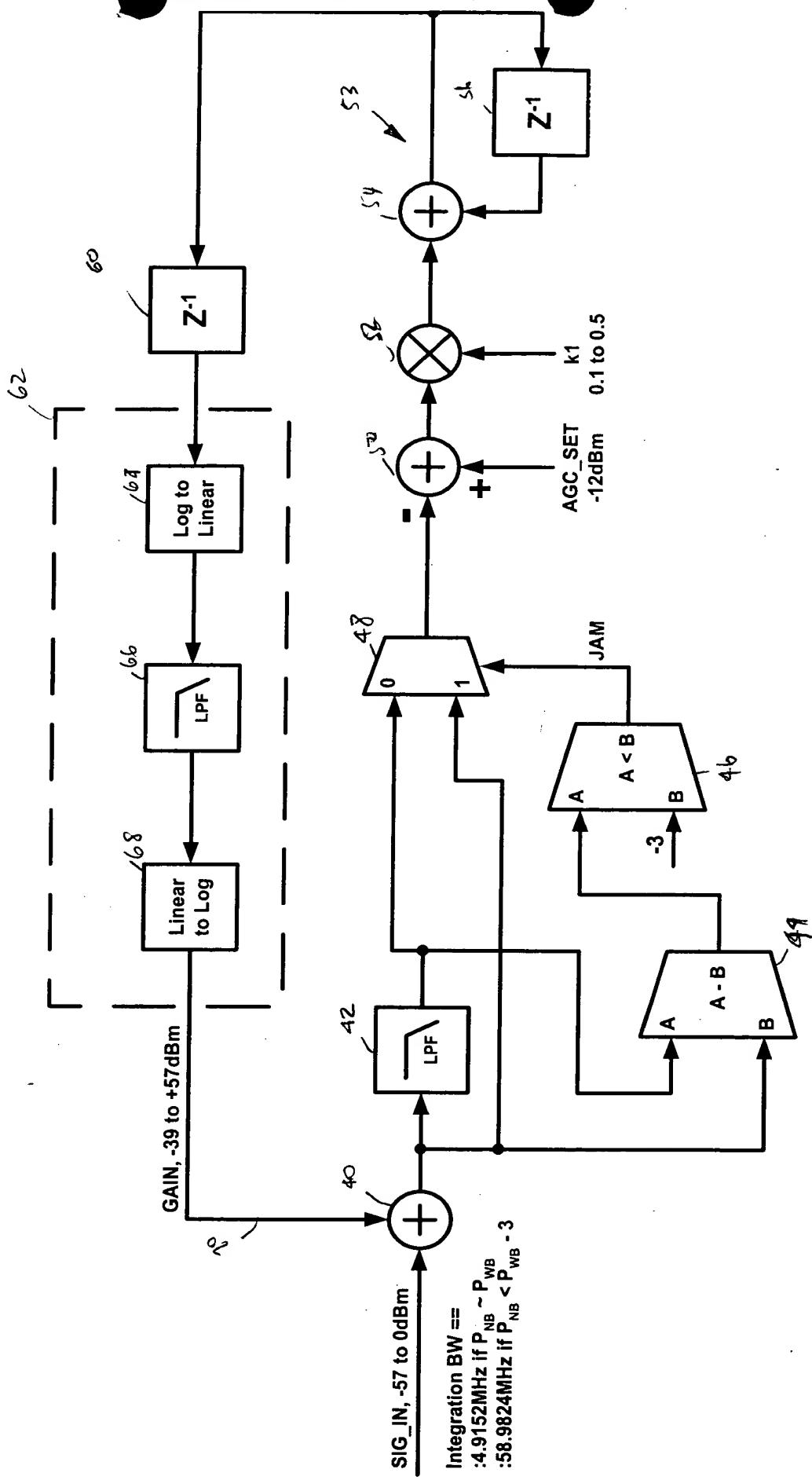


FIG. 4

This section is controlled by a 1/32X clock.

For simplification purposes, this gain block is simulated (in Matlab) with only one gain control signal and one lumped gain VGA.

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CIC gain values (based on decimation and expected input levels). See AD666 data sheet for details.

ADC: 12bits, 58.9824MS/S @ 70MHz IF, 2Vpp
AD6620 Output: 16bits (I&Q), 4.9152MS/S @ Baseband
AGC Rate: 38.4kHz

Below are block diagrams for the CIC filters (actual implementation), however, for simulation simplicity, they can be realized using the following

Fix implementation:

$$h2 = [1 2 3 2 1] / 16$$

$$h5 = [1 5 15 35 65 101 185 155 155 135 101 65 35 15 5 1] / 1024$$

Note that the appropriate scale values (S2 and S5) are included in the above coefficients, but not in the block diagrams below. In the block diagram case, the scale PRECEDES the filter (to prevent overflow).

Also, the RCF filter is a simple 12 tap FIR with the following coefficients:

NOTE: The log table block includes a priority encoder and other logic to properly address the table.

CIC5 Block Diagram

CIC2 Block Diagram

NOTE: The Inverse log table block includes logic to properly address the table.

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This section is controlled by a 1/32X clock.

Since the gain control voltage is linear, filtering the RMS power in dB is possible. Otherwise, the data would need to be converted to volts prior to integrating.

Based on decimation (four levels), See AD6620 details

This section is controlled by a 48X clock.

This section is controlled by a 1/32X clock.